Customer No.: 31561
Docket No.: 11555-US-PA
Application No.: 10/605,099

AMENDMENTS

In The Specification

Please amend paragraph [0037] as follows:

[0037] However, for the large block flash memory, this pipeline design in FIG. 7 can be combined with the mechanism shown in FIG. 6. FIG. 8 is a drawing, schematically illustrating another programming method to memory cell array of the large block flash memory in sequence, according to an embodiment of the invention. In FIG. 8, four [[~~blocks~~]]sectors as a page [[~~is~~]]are sequentially sending between the host and the controller as well as between the controller and the flash memory. After, i.e., the page 0 data is completely received at the data cache 302, the command "15H" is issued at (B) instead of the command "10H" in FIG. 6. Here, the command "15H" in function with the start program command "10H" is also called as a "start program with data cache" command. Then, the data in data cache is shifted to the page buffer 304. At (C), when parts of one page data are transferring between the host and the controller, parts of the same page data are moving into the data cache 302 within flash memory. At the same time, the previous one page stored in the page buffer 304 is programming into the memory cell array 306. At (D), after the controller sends the 15H command to flash memory, the page 1 data is moving from the data cache to page buffer. At the same time, the controller still can be receiving page 2 data from the host. Therefore, the busy time between two pages is, for example, about 2 microseconds but not the 200 microseconds (see RY/~~bar(BY)~~ $\overline{BY}$ signal, ~~wherein bar () represents an inverse state.~~). When the last page is received, the "10H" command can be issued at (F).